

PERSONAL INFORMATION

Name **FAROOQ ANWAR SHEIKH**
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WORK EXPERIENCE

- Duration **JANUARY 2022- TILL DATE**
- Name and address of employer **IMEC, Eindhoven, Netherland**
- Type of business or sector Radio Technology
- Occupation or position held Hardware Design/Verification Engineer
- Main activities and responsibilities
 - ◆ Hardware Implementation in SystemVerilog/VHDL for Ultra Wideband system modules, like PSI interface, CFO estimator, Debug Module.
 - ◆ Hardware Verification in SystemVerilog for Ultra Wideband system with Models in Matlab.
 - ◆ Hardware porting of UWB to Xilinx FPGA and debugging in lab with Xilinx Lab tools.
- Technologies VHDL, System Verilog, ASIC(TSMC), Cadence Xcellium, Xilinx FPGA., Constraint based verification.

- Duration **FEBRUARY 2016- DECEMBER 2022**
- Name and address of employer **Elmos Semiconductor, Dortmund, Germany**
- Type of business or sector Automotive
- Occupation or position held Hardware Design/Verification Engineer
- Main activities and responsibilities
 - ◆ Hardware Verification of Halios Gesture Control with System Software and UVM.
 - ◆ RTL implementation in VHDL for "AIRBAG SYSTEM" specifically SPI, JTAG, Safing Agent, Configuration, Supply and GPO. Also Implemented individual UVM Environment for the above modules to verify.
 - ◆ Hardware Design and implementation in System Verilog for "USPA hardware" specifically ADA (Analogue to Digital converter) and OTP memory. ASIC design on ELMOS Technology and prototyping in FPGA.
- Technologies VHDL, System Verilog, ASIC(TSMC, ELMOS), VCS, Synopsys Design flow. Xilinx FPGA. UVM, Assertion, Constraint based verification, TLM, checker, Driver.

- Duration **OCT 2012 – SEPTEMBER 2015**
- Name and address of employer **[dSpace Gmbh, Paderborn, Germany](#)**
- Type of business or sector Automotive
- Occupation or position held Consultant as a Software/Hardware Design Engineer. (Main Employer Green Digit)
- Main activities and responsibilities
 - ◆ RTL implementation of Partial Configuration (ICAP) of Dspace Debug module in VHDL, for Xilinx Kintex-7 FPGA.
 - ◆ Developed and implemented in C, Autosar Ethernet Drivers for embedded HIL systems.
 - ◆ Implemented Matlab Simulink models and code generator for Dspace Autosar product.
- Technologies VHDL, Xilinx Vivado, Xilinx Plan Ahead, AUTOSAR. C/C++, RTOS(Qnx, Debian), Linux Kernel, Static Libraries, Dbus, Matlab. Embedded Systems. TCP/IP, UDP, DOORS.

- Duration **APRIL 2012 – AUGUST 2012**
- Name and address of employer **[Infineon Technologies, Duisburg, Germany](#)**
- Type of business or sector Chip Manufacturers.
- Occupation or position held Consultant as a Mixed Signal Verification Engineer. (Main Employer Green Digit)
- Main activities and responsibilities
 - ◆ I/O-Pads and oscillator verification and validation in C65 and L90 Technology.
- Technologies Avenue, Cadence Virtuoso, Cadence Virtuoso Analog Design Environment, Linux Shell scripting, Pspice.

- Duration
- Name and address of employer
 - Type of business or sector
 - Occupation or position held
- Main activities and responsibilities
- Technologies

NOVEMBER 2011- OCTOBER 2015

[Green Digit Gmbh, Gilching, Germany](#)

Engineering Service Provider.

Hardware Design/Verification Consultant.

- ◆ In house Project: Development in C Temperature SMS based alarm system for ARM processor.
- ◆ **Consultant:** Worked with Infineon and Dspace as a Consultant. Details are listed above. Verilog, Xilinx Spartan2/ Vertex 2 FPGA, Matlab, Modelsim .

STUDENT EXPERIENCE

- Duration
- Name and address of employer
- Main activities and responsibilities
- Technologies
- Duration
- Name and address of employer
- Main activities and responsibilities
- Technologies

MAY 2011 – OCT 2011

[GlobalFoundries Inc, Dresden Germany](#)

Internship.

- ◆ Automated Static/dynamic Power and EM/IR flow for Analogue/Digital and Mixed signal SOC in 28 and 20nm Technology.
- TCL and Shell scripting. GDS-2 and LEF/DEF layouts, Apache Redhawk, Apache Totem, Cadence Virtuoso, Synopsys StarXT, Calibre DRV, Hspice, Spectre,

JUN 2010 – APR 2011

[Vodafone Chair Mobile Communications, Dresden Germany](#)

Internship.

- ◆ RTL Hardware Implementation (in Verilog) and verification of Reed Solomon (RS) and BCH encoder/decoder for Altera FPGA. Development in C, verilog Code generator that generates RS/BCH encoder decoder.
- Verilog, Altera Stratix 2 GX FPGA, Timing and Area Constraints, Avalon standard, Ethernet IP, HIL, Quartus 2, Modelsim, Matlab.

EDUCATION AND TRAINING

- Duration
- Name and type of organization providing education and training
 - Principal subjects
- Title of qualification awarded
 - Final Year Project
- Duration
- Name and type of organization providing education and training
 - Principal subjects
- Title of qualification awarded
 - Final Year Project

Oct 2008 –March 2011

[Lund University, Lund, Sweden](#)

- ◆ Chip Design, Digital Signal Processing, Embedded Systems, Algorithms in Signal Processing. A/D convertors. Analogue Design. Adaptive signal processing.
- M.Sc., System on Chip
- RTL based Hardware Implementation (in Verilog) of RS encoder/decoder and BCH encoder/decoder.

JUNE 2002 –APRIL2006

[Comsats University, Islamabad, Pakistan](#)

- ◆ Electrical Engineering, Digital Signal Processing, Embedded Systems, Software engineering.
- ◆ Circuit design. Processors and telecommunication.
- B.S. Electrical and Computer Engineering
- RTL based Hardware Implementation (in Verilog) of Least Mean Square Adaptive Filter using Distributive Arithmetic's.

PERSONAL SKILLS AND COMPETENCES

- Reading skills
- Writing skills
- Verbal skills

English (Fluent)

Excellent
Excellent
Excellent

German (B1 Level)

Intermediate
Intermediate
Good

TECHNICAL SKILLS
AND COMPETENCES

*Acquired in the course of life and
career but not necessarily covered
by formal certificates and diplomas.*

Hardware

- VHDL/ System Verilog/Verilog.
- FPGA/ASIC.
- UVM Verification flow.
- Validation (SET system) ..

Embedded Systems

- ARM CORTEX M0 .
- 6 bit H430 Microcontroller
- C/C++ Development for RTOS(QNX, Debian, TS-Linux)
- Microblaze from Xilinx.
- Bus Systems(Ethernet, SPI, Safespi, I2C ICAP, JTAG)

Programming Languages

- VHDL/ System Verilog
- C/C++
- Matlab
- Automake/Make scripting
- Perl/Ruby
- TCL / Shell scripting

Tools

- HDL Simulator(Modelsime, VCS)
- Xilinx(ISE, EDK, XPS, PlanAhead, SDK, IP Generator, Chipscope Pro, System Generator)
- Quartus 2(IDE, Memory Content Editor, Signal Tap2 Logic Analyzer)
- Apache (Totem, Redhawk)
- Matlab(Simulink, HDL Code Designer).
- Automake, Qmake, Cmake
- QNX Momentics, Eclipse, Emacs
- Microsoft (Visual Studios, Office, Windows)

ORGANISATIONAL SKILLS
AND COMPETENCES

- Have contributed in opensource society for both Hardware (opencorse.org) and software.
- Always had been contributing for developing community with helping developers in different forums.